CLAIMS:

1. A semiconductor device including:

a semiconductor substrate;

a plurality of circuit regions formed on a device formation region in said semiconductor substrate, and having gaps of 0.1 to 125 μm between them; and

device isolation regions so formed as to isolate a plurality of circuit regions from one another on said semiconductor substrate, and having a width of 0.1 to 2.5 μm;

wherein a ratio of the width of said device isolation region to the width of a plurality of said circuit regions adjacent to said device isolation region is from 2 to 50.

2. A semiconductor device according to claim 1, wherein said device isolation region is a groove formed in said semiconductor substrate by etching a portion, among a pad oxide film formed on the surface of said semiconductor substrate and a nitride film formed on said pad oxide film, existing on said device isolation region, and a depth of said groove measured from the position of said pad oxide film on said semiconductor substrate is from 0 to 10 nm.

3. A semiconductor device according to claim 2, wherein said groove has a thermal oxide film formed by thermal oxidation, and a formula relating to a dislocation occurrence limit stress value resulting from thermal oxidation in said device formation region and

said device isolation region adjacent to one another is established:

$$\sigma/\sigma_c = [\{0.78 + 0.054D - 0.00086D^2\} + \{-0.040t_p + 0.00086t_p^2\} + \{-0.01t_n + 0.000051t_n^2\}] \times [0.043 + 0.61L - 0.14L^2 + 0.015L^3] \times [1.4 - 0.49S + 0.18S^2 - 0.021S^3] \leqq 1$$

where t_p is the thickness of said pad oxide film, t_n is the thickness of said nitride film, and D is the depth of said groove.

4. A semiconductor device according to claim 3, wherein a stress occurring in the proximity of said groove due to said thermal oxidation is analyzed by a finite element method inclusive of numerical analysis from the thickness and the internal stress of said nitride film, the thickness of said pad oxide film, the depth of said groove, the width of said device isolation region, and the width of said device formation region adjacent to said device isolation region.

5. A semiconductor device according to claim 1, which further includes:

a memory circuit formed on said device formation region; and

a peripheral circuit formed on said device isolation region and connected to said memory circuit; and

wherein a ratio of the width of said device isolation region to the width of a plurality of said

circuit regions adjacent to said device isolation region is a value in said peripheral circuit.

6. A semiconductor device according to claim 5, wherein the width of said device formation region in said peripheral circuit is not greater than 5 μm.

7. A semiconductor device according to claim 1, wherein the width of said device isolation region is not smaller than 3 μm, and the width of said device formation region is from 0.1 to 1.0 μm.

8. A semiconductor device according to claim 7, wherein said device isolation region is a groove formed in said semiconductor substrate by etching a portion, among a pad oxide film formed on the surface of said semiconductor substrate and a nitride film formed on said pad oxide film, existing on said device isolation region, and the depth of said groove measured from the position of said pad oxide film is from 0 to 10 nm.

9. A method of designing a semiconductor device, comprising:

a step of measuring a thickness of a pad oxide film formed on a surface of a semiconductor substrate and a thickness of a nitride film formed on said pad oxide film;

a step of measuring an internal stress of said nitride film;

a step of measuring the width of a device formation region formed on said semiconductor substrate

and a width of a device isolation region adjacent to said device formation region;

a step of measuring a depth of a groove formed inside said semiconductor substrate by etching a portion existing on said device isolation region among a nitride film formed on said oxide film;

a step of conducting stress analysis using said thickness, said width, said depth and said internal stress and obtaining an internal stress estimated to occur due to thermal oxidation in the proximity of said groove;

a step of preparing a design chart representing a region in which a quotient obtained by dividing said stress by a dislocation occurrence limit stress, at which dislocation occurs due to thermal oxidation, exceeds 1, by using the width of said device formation region and the width of said device isolation region as parameters; and

a step of setting a value of the width of said device formation region and a value of the width of said device isolation region, at which dislocation does not occur, in design of said semiconductor substrate.

10. A method of designing a semiconductor device according to claim 9, wherein said groove has a thermal oxidation film formed by thermal oxidation, and which further includes:

a step of applying data of said design chart so as to establish the following formula relating to a

dislocation occurrence limit stress value due to thermal oxidation in said device formation region and said device isolation region adjacent to one another:

$$\sigma/\sigma_c = [\{0.78 + 0.054D - 0.00086D^2\} + \{-0.040t_p + 0.00086t_p^2\} + \{-0.01t_n + 0.000051t_n^2\}] \times [0.043 + 0.61L - 0.14L^2 + 0.015L^3] \times [1.4 - 0.49S + 0.18S^2 - 0.021S^3] \leqq 1$$

wherein L/S in a value of said ratio, t_p is the thickness of said pad oxide film, t_n is the thickness of said nitride film and D is the depth of said groove.

11. A method of designing a semiconductor device according to claim 9, which further includes:

a step of deciding an etch-back distance of said pad oxide film not causing the occurrence of dislocation by using said design chart; and

a step of etching and removing said pad oxide film by said etch-back distance in a direction parallel to the surface of said semiconductor substrate.

12. A method of designing a semiconductor device comprising:

a step of measuring a thickness of a pad oxide film formed on a surface of a semiconductor substrate, and a thickness of a nitride film formed on said pad oxide film;

a step of measuring an internal stress of said nitride film;

a step of measuring a width of a device formation region formed on said semiconductor substrate, and a width of a device isolation region adjacent to said device formation region;

a step of measuring a depth of a groove formed in said semiconductor device by etching a portion of said nitride film formed on said pad oxide film and existing on said device isolation region;

a step of conducting stress analysis by using said thickness, said width, said depth and said internal stress, and obtaining an internal stress estimated to occur due to thermal oxidation in the proximity of said groove;

a step of preparing a stress distribution chart representing a region, in which said stress exceeds a dislocation occurrence limit stress at which dislocation occurs due to thermal oxidation, by using the width of said device formation region and the width of said device isolation region as parameters; and

a step of setting the width of said device formation region and the width of said device isolation region not causing dislocation by using said stress distribution chart in designing said semiconductor substrate.

13. A semiconductor fabrication apparatus comprising:

means for measuring a thickness of a pad oxide film, a thickness of a silicon nitride film, and

internal stress of said silicon nitride film, respectively;

an arithmetic unit for conducting numerical analysis by using said measurement values, a design value of a width of a device formation region and a design value of a width of a device isolation region adjacent to said device formation region; and

display means for displaying a design chart representing a region in which an internal stress occurring around said device isolation region due to selective oxidation exceeds a limit value by using said film thickness and said width as parameters;

said apparatus deciding a substrate groove formation depth at the time of removal of said silicon nitride film before selective oxidation.